REMARKS

The present amendment is in response to a couple of communications received subsequent to the previous response submitted on October 21, 2003, via facsimile, which due to the time difference between the source of the transmission (Libertyville, IL) and the destination of the transmission (U.S. Patent and Trademark Office), was received on October 22, 2003, which is entitled to have been timely received relative to an October 21, 2003, term date. The couple of communications received subsequent to the previous response included a communication received via mail dated November 4, 2003, and a courtesy copy of a further communication received via facsimile on November 19, 2003, which communicated the withdrawal of the previous communication, and established a one month term for more fully responding to the Office Action dated May 21, 2003.

The latter of the two subsequent communications was received after a telephone interview between Examiner Thai, and applicants' undersigned representative, Lawrence Chapa. During the telephone interview, the determination of non-responsiveness of the prior response was discussed, and a request for reconsideration was made as to the communication mailed November 4, 2003. The nature of at least some of the amendments was briefly discussed. Most notably the amendments to claim 1, which included the incorporation of at least some of the elements from claims 2-4, as well as additional amendments including the claimed relationship (i.e. distinction) between a first shared bus connection and a second shared bus connection.

The present response more fully responds to the prior Office Action, highlighting in greater detail the specific language in the claims, believed to distinguish the present claims from the cited references.

Substantively, the present amendment is in response to the Official Action dated May 21, 2003, wherein the Examiner rejected pending claims 1-16 and 29-34. More specifically, claims 1-14 are rejected as being anticipated by Heath et al., US Patent No. 4,901,234; claims 29-34 are rejected as being anticipated by Garde et al., US Patent No. 5,634,076; and claims 15 and 16 are rejected as being unpatentable over Heath et al., '234, in view of Kamiya, US Patent No. 5,809,335. In the present amendment, claims 2-4, 17-28, 30 and 35-37 have been canceled, and claims 1, 5-16, 29 and 31-34 have been amended.

As presently amended, the claims highlight a data transfer system and corresponding method having a direct memory access element including multiple data busses or interfaces, associated with multiple memories and or processors, and a plurality of node, which in at least some embodiments are associated with a plurality of peripherals. The direct memory access element is programmable and/or is adapted for configuring direct memory access data channels to enable the transfer of data between the plurality of nodes and one or more of the elements associated with the multiple interfaces and/or data busses. None of the references cited teach or suggest the use of a programmable and/or configurable direct memory access system, which provides reconfigurable direct access between at least three groupings of elements.

More specifically, claim 1 provides for at least three groupings of elements between which the programmable direct memory access module allows for reconfigurable direct memory access. The three groupings of elements include a plurality of peripheral interfaces, a first shared bus connection (associated with both the first memory and the first processor), and a second shared bus connection (associated with both the second memory and the second processor). At least one example of the same is highlighted in FIG. 1 of the present application. Alternatively Heath et al., U.S. Patent No. 4,901,234, has only two groupings of elements (i.e. the peripherals associated with the family bus, and the system elements including the CPU 10, math co-processor 14 and main memory 15 associated with a single common system bus).

Claim 9, similarly focuses on multiple element groupings associated with multiple interfaces. More specifically, claim 9 includes a direct memory access controller having a first interface associated with a first memory, a second interface associated with a plurality of nodes (which in at least one embodiment are associated with a plurality of peripheral interfaces e.g. see claim 10), and a third interface associated with a second memory. For the same or similar reasons noted above, relative to claim 1, claim 9 is distinguishable from Heath et al., '234, which does not similarly support the three different interfaces, two of which are associated with a corresponding memory, and a third which is associated with the plurality of nodes between which communication with at least one of the memories is selectively established via the direct memory access controller.

Similar reasoning is relevant with respect to claims 12 and 29, which similarly includes a first, second and third interface (claim 12) or a first and second processor direct memory access

interface, and one or more peripheral ports, as well as associated first and second data bus (claim 29). Relative to claim 29, Garde et al., U.S. Patent No. 5,634,076, fails to be associated with multiple data buses.

Because the dependent claims are dependent upon a base claim, which is allowable for the reasons noted above, the dependent claims should be found to be similarly allowable.

The applicants contend that the claims, as presently amended, are allowable over the prior art of record, for the reasons noted above. Allowance of the application is therefore respectfully requested. Should any issues remain unresolved after the consideration of the present response, the Examiner is invited to contact the applicant's representative at the number listed below to discuss the same.

Respectfully submitted,

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